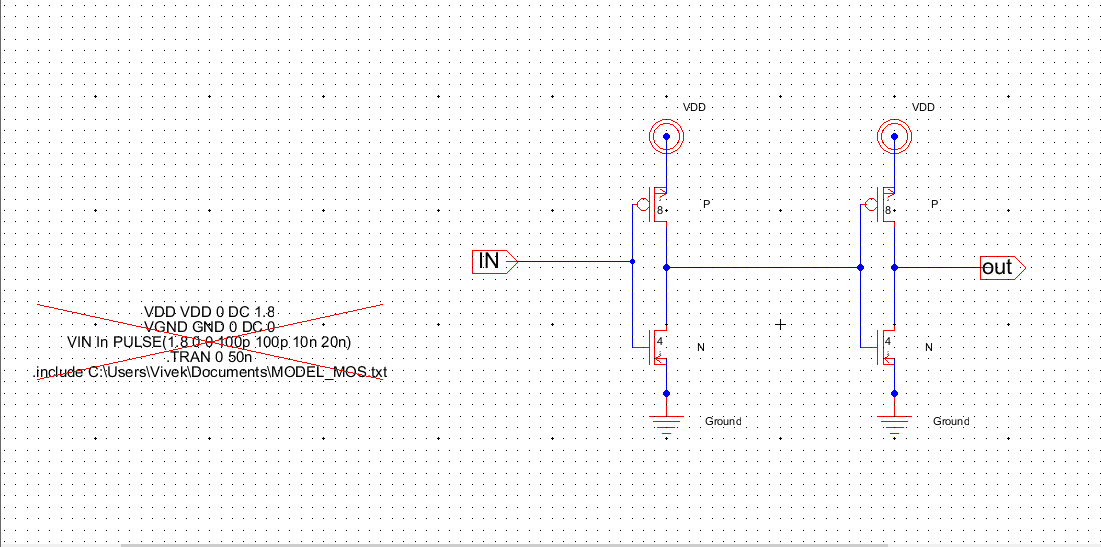
**EE 457 Homework#3**

Problem 1

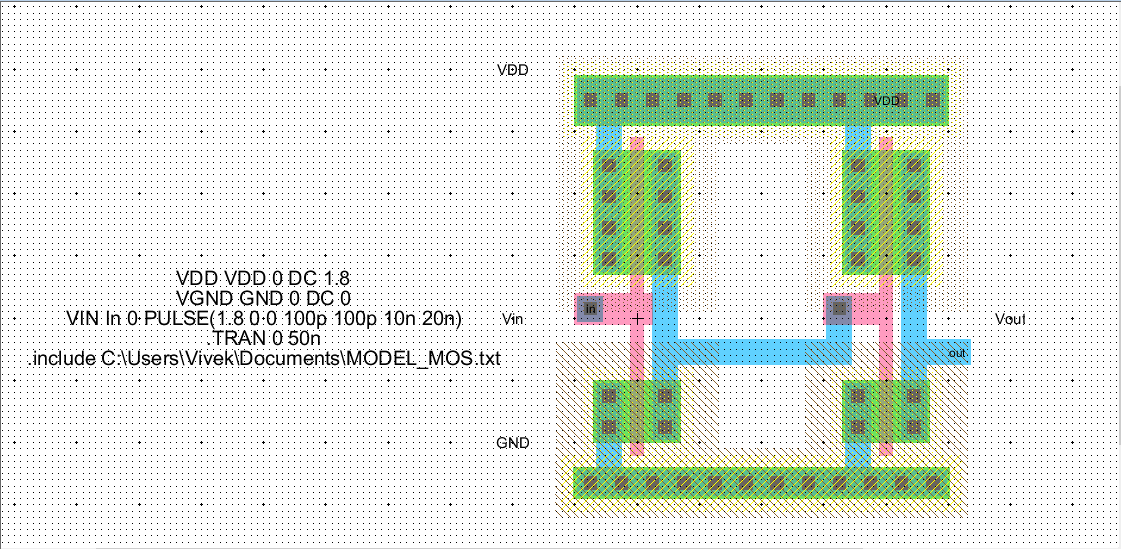
Design a series of two CMOS inverters and do layout using Electric to match rise and fall times from calculations you

performed in HW#2. Perform DC simulations to verify circuit operation. Provide the following screenshots:

1. Draw a series of two CMOS inverter schematic in Electric. Print out the schematic.

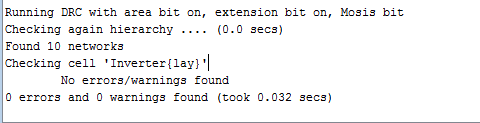


2. Layout the CMOS inverters. Make the PMOS twice the size of NMOS. Print out the layout with grid.



3. Perform a Design Rule Check (DRC) and ensure all design is validated. Print the screen to

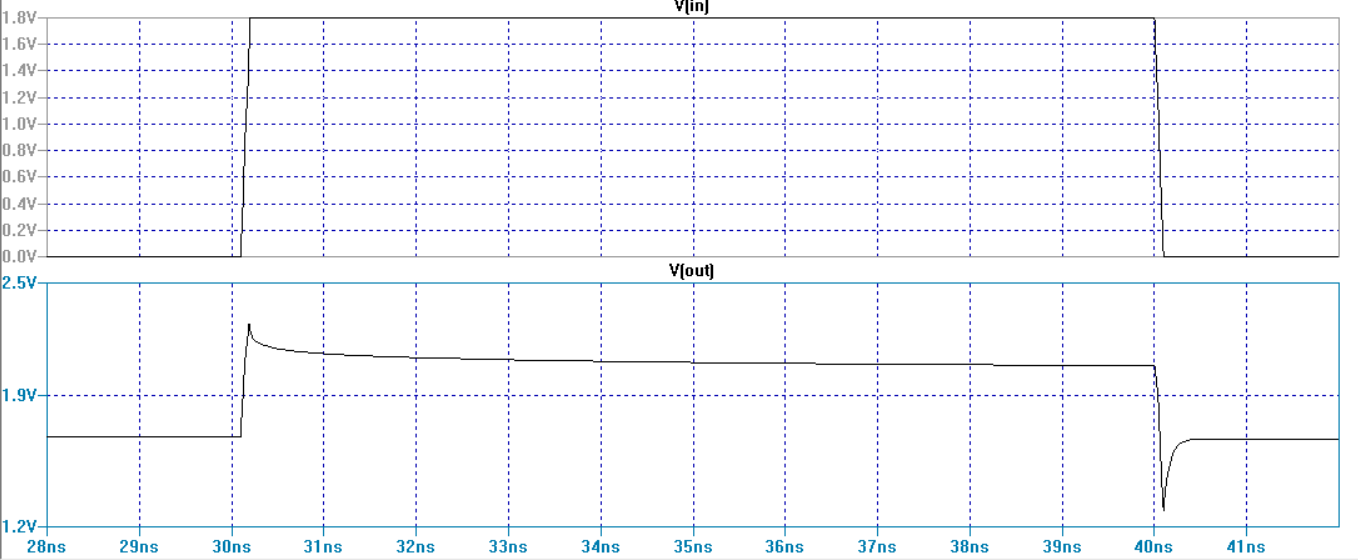
indicate no DRC errors.



4. If you have successfully performed extraction of the layout, provide simulation of the RC

network of PMOS and NMOS to perform SPICE simulation of rise and fall times. Measure rise

and fall time delays and provide them in a table form. Print out the pulse input and output.



|  |  |  |  |
| --- | --- | --- | --- |
|  | Homework # 2 | Homework #3(simulations) | Difference in them |
| Rise time | 2.8864ns | .30ns | 2.5864 |
| Fall time | 8.812ns | .43ns | 8.382 |

5. Can you suggest the perfect size of NMOS and PMOS to match the rise and fall times?

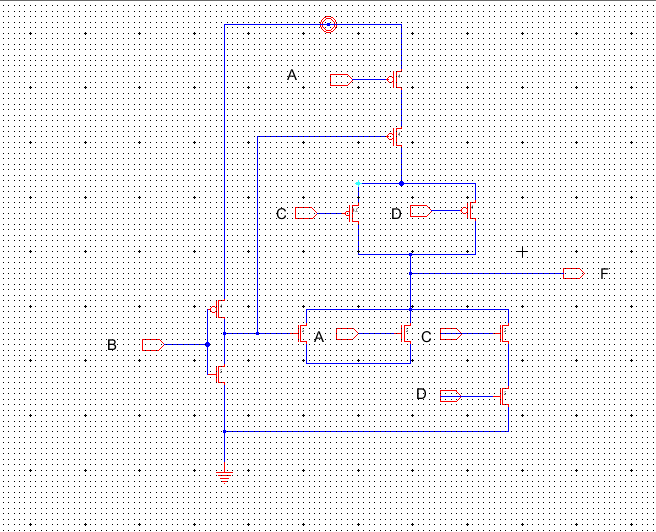
Note: Make sure the background is white and Vin & Vout waveforms are dark enough to print.

PMOS Length = 0.7µm Width 7µm

NMOS Length = 0.7µm Width 3.5µm

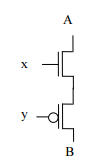
Problem 2

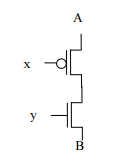
Design the CMOS logic gate for the function  .

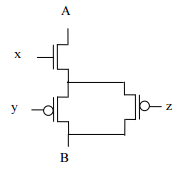


Problem 3:

Each MOSFET shown below has an input of a 0 or a 1. For each circuit, determine the Boolean expression of the output B in terms of the inputs shown in each circuit.

a)  **B = x \* ~y**

b)  **B = ~x \* y**

c)  B = (x \* ~y\* ~z) + (x \* ~y\* z) +(x \* y\* ~z)

B = x\* {(~y\* ~z) +(~y\* z)+ (y\* ~z)} //Distributive Law

**B = x\* (~y + ~z)** //Complement Law

Problem 4:

Go to http://cmosedu.com/videos/electric/electric\_videos.htm. Watch Videos #3, #4, and #5. Please review tutorial #3 and #4, if you have not watched it last week. Write some key salient features about each video in your own words for videos #3, #4 and #5, and tutorial #3 and #4.

Video # 3)

One of the features that I thought that was important was "export", we can export particular inputs and outputs instead of sending the entire inputs and outputs. This is very convenient when testing particular aspects of your design. Another aspect that I find it important is creating cells after we design a circuit with transistors, now we can have these circuits in a cell design more complex circuits.

Video # 4)

The 3d view of the circuit design that we created. It is important that we can see the simulation of how the design looks in real life.

Video# 5)

In this video, he shows how to setup multiple inverter cells in series connection and how to create bus wire to connect the inputs and outputs of those inverters. It is very important understand how to send multiple signals into a design for a desired output.